

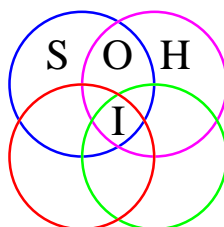
**OMI small
demonstrator
projects for SMEs
(task 5.16)
Proposal**

ESPRIT

Small demonstrator of OMI and HIC

Integration

SOHI



“Supporting the growth and the spread of the Information Society”

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Part 2: Description of SOHI Project

1.1 Technical Summary

1.1.1 What

- To demonstrate best practice for an SME in development of boards and chips, seen as Requirements capture → PLD/FPGA → PCB → proven PCB → modified PLD/FPGA → Conversion to small ASIC → Revised PCB with ASICs.
- To demonstrate integration on PCB of an OMI core processor with an OMI Real-time Operating System and with OMI HIC communications.
- To demonstrate the hardware routing capability of OMI HIC (IEEE 1355) with components whose continued supply is assured, whose cost demonstrates the exceptionally low cost for technology of comparable performance.

1.1.2 Why

- To go some way to fill the gap left by the failure of SGS-THOMSON to exploit the HIC/1355 technology by providing components so that their partners and others who have invested a total of probably over 50MECU can themselves exploit the technology.
- To build the proposer's business by improving on existing board and chip products, by proving the IPR embodied in the chip design (currently a programmed PLD), and by demonstrating response in these products to customer needs.

1.1.3 Who

- SOHI is proposed by 4Links for technical help, a UK SME specialising in 1355 and offering boards, chips, IPR and consultancy for 1355 links.

1.2 Project Objectives and Scope

1.2.1 Objectives

- To demonstrate best practice for an SME in development of boards and chips, seen as Requirements capture → PLD/FPGA → PCB → proven PCB → modified PLD/FPGA → Conversion to small ASIC → Revised PCB with ASICs.
- To demonstrate integration on PCB of an OMI core processor with an OMI Real-time Operating System and with OMI HIC communications.
- To demonstrate the hardware routing capability of OMI HIC (IEEE 1355) with components whose continued supply is assured, and with the HIC links able to operate with performance close to their capability.
- Quantitative objectives of this project are therefore:
 - To achieve average latency of communication of less than 10 microseconds per hop (i.e. if the packet travels on four links between two nodes via three switches, the latency should average less than 40 microseconds);
 - To achieve a reasonable proportion of PCI throughput with an aim of sustained throughput of at least 20Mbytes/s and hopefully higher than this, with a total throughput through the switch around 40 Mbytes/s (50% utilisation of four 100 Mbit/s external ports);
 - To achieve an integrated component for a 1355 port with a unit cost price to 4Links of well under \$5, and with a target cost of \$3, and with performance at least 100Mbits/s and power consumption considerably lower than the several Watts of the STC101 or the 1 Watt of the programmed PLD, with a target dissipation of no more than 500mW.
- Qualitative objectives are:
 - To prove the logic design of a small hardware routing switch between ports of IEEE 1355 and an additional port to PCI
 - To prove the design of an interface between a core processor and 1355 links, as a feasibility study for a possible chip development of integrating 1355 links with the ARM processor
 - To have a small chip built as a PLD/FPGA conversion which proves the design process of Requirements capture → PLD/FPGA → PCB → proven PCB → modified PLD/FPGA → Conversion to small ASIC → Revised PCB with ASICs.
 - To use these chips at least partially to fill the gap left by SGS-THOMSON's withdrawal from the market for HIC/1355 components.

It is not an objective of initial PCB to achieve a minimum cost implementation. For the revised PCB with the small ASICs, cost will be substantially reduced, but again, absolute minimum cost is not required. For markets such as Space and fault-tolerance, the cost is less important than for very high volume markets. For communications and database systems, the cost of alternative switch technology is also high. For volume applications, the PLD/FPGA conversion would be a larger integration, which will benefit from the experience on this project of a deliberately limited scale of integration.

1.2.2 Technical State of the Art

The major benefits of IEEE 1355/HIC are low-latency communications, scaleable growth in system throughput while maintaining 60% or greater link utilisation at each node, cost effective hardware switch technology, very low cost (logic of the same order as a 16550 UART), and simple fault-tolerance resulting from the redundant connections inherent in any multi-dimensional network. Alternative, competing, technologies based on bus and ring topologies, such as SCI and 1394 FireWire, do not scale in that a network of ten nodes can only maintain an average throughput of 10% or less at each node (or 1% for 100 nodes), and these one-dimensional topologies are inherently liable to single points of failure. Other switched technologies such as FibreChannel and ATM need more complicated protocols which result in more expensive switches and increased latency, so that 1355 is being used inside switches for these technologies.

Boards exist to demonstrate 1355 which are based on components from SGS-THOMSON Microelectronics (STM) which have either been withdrawn or which are threatened with cancellation. Boards using the T9000 offer reasonable bandwidth, but suffer from performance of the memory bus, restrictions on packet length and protocol, and bugs in the silicon which have caused the withdrawal of the product. The STC104 is currently the only switch available for 1355 DS-DE links, and at 32 ports does demonstrate the high valency possible for a 1355 switch. But many users do not need so many ports, bugs in the STC104 prevent its being used to demonstrate fault-tolerance, and the low sales resulting from the large size and from the bugs are threatening its existence.

4Links has an existing PCI board product for 1355 which does not use these components, and also has as a product a link macrocell for 1355 which fits a small PLD. Without this experience and these products, the scope of this project would be more than 4Links could manage, but by building on this foundation the project is an achievable challenge.

The embedded operating system Virtuoso provides a view of a network of many processors as a virtual single processor, and manages all the network communication and routing between the processors. Virtuoso runs on a variety of processors including the ARM. Because of the appropriateness of 1355, Eonic Systems, the owners of Virtuoso, have been keen to promote 1355. The routing between processors in Virtuoso is currently store-and-forward by the processor, and this project exploits the simplicity of hardware routing with 1355 to provide Virtuoso with lower latency and reduced processor load as well as the fault-tolerance required.

Perhaps the over-riding reason for choosing the processor is the long term one of which processor would be ideally integrated with 1355 links. The Intel family of processors is attractive except that there are very few manufacturers and these manufacturers do not tend to be interested in custom variants. The processor that is made by the largest number of different silicon vendors is probably the ARM, which also turns out to be an excellent technical choice for this project, as well as supporting the thrust of this project in integrating different OMI technologies. Technically, the ARM is useful in having a well designed memory interface, and in having a fast response to interrupts, and it has been seen to be used in similar applications to good effect.

1.2.3 Methodologies to be used

The proprietor of 4Links has a long experience of requirements capture for product definition, with particular success in this for the TRAM family of transputer modules. Recent work in other industries for requirements capture has used Quality Function Deployment, or the “House of Quality” to tabulate customer and user requirements and relate these to technology choices. These techniques do not give the answers, but they provide a focus on customer needs and a more or less quantitative basis for trade-offs between design choices. While the overall project has been formulated with the experience of synthesising a single solution to meet many diverse requirements, and before 4Links was fully aware of the HoQ techniques, these techniques will be used to refine details within the design. The techniques are expected not only to improve the design but to strengthen 4Links experience of the techniques in product definition.

4Links currently produces boards with CPLDs and other components, and also sells programmed CPLDs which, together with a couple of FIFOs, implement a 1355 interface. The choice of CPLDs and separate FIFOs was partly on the basis of cost of the components, but more on the cost of the development tools for FPGAs that can integrate the logic and FIFOs.

To develop more integrated implementations, it is necessary to move towards FPGAs or at least to more generic tools that can be used with a variety of different families of CPLD and FPGA. Tools will be bought, therefore, to develop FPGAs as well as CPLDs, and to simulate collections of these devices used together in a system.

With several ports in the routing switch, with the interface to the core processor, and with the interface to PCI, there is scope to integrate all this logic into a single FPGA or CPLD, and to convert this design to a single ASIC. That would produce a rather specialised product, however, would be far more expensive in terms of both NRE and unit cost than a smaller chip, and would carry far more risk than taking a smaller chip to ASIC. So the project will demonstrate the process of converting FPGA/CPLD designs to ASIC, but on the basis of one or two ports only, with the target of minimising the cost of the chip and the risk of the conversion.

The practice of proving the logic design on a printed circuit board which is used for applications is sometimes avoided because it is possible fully to simulate the logic design. Best practice, however, is not only to prove that the design is a correct implementation of the specification, but that the specification is actually what the users need. So the step of proving the design on a prototype PCB is seen as an essential part of the best practice demonstration of this project.

1.3 Industrial relevance and impact on society

1.3.1 Industrial context

There is currently an explosion of interest in serial interfaces, all of them designed for a particular application, and all of them trying to remove some of the limitations imposed by the conventional bus. Examples are ATM, FibreChannel, IEEE 1394 FireWire, SCI, SSA, and the recent developments of Ethernet.

IEEE 1355 is both the same and different. It is the same in being a fast serial interface, and in using point-to-point links. It is different in having exceptionally low silicon implementation cost (about the same logic as a 16550 UART, but capable of 100 to 200 Mbits/s, with the same packet protocols extending to several Gbits/s). It is different in that this low silicon cost and protocols designed for switching make it possible and inexpensive to incorporate switching at every multi-port node. So traffic does not need to visit every node in the network and so the rest of the network is free for other traffic, giving improvements in security, latency, and network throughput. The switches make it inexpensive to build networks with connections in multiple dimensions, drastically reducing the path length between different nodes in the network and providing an inherent redundancy for fault-tolerance.

1355 is also different in being designed as a heterogeneous interconnection between microprocessors, rather than being designed for any particular application. As almost every piece of electronic equipment nowadays includes a microprocessor or a microcontroller, an interface designed for connecting microprocessors and microcontrollers must be appropriate compared with any interface just designed for a single application.

Partly because particular industry groups tend to own an interface designed for their application, partly because of bugs, delays, and a lack of marketing from the originating chip supplier, 1355 has lost ground to some of the other serial interfaces. The breadth of applications, however, for which it has been adopted by niche segments of the markets, show its value.

1.3.2 Market opportunities and segmentation

The European Space Agency has adopted 1355, for one spacecraft at least, and potentially for several more technology trials, as greatly simplifying and reducing weight in spacecraft. Independently of ESA, two major contractors to ESA adopted 1355, not only as ideal for the spacecraft, but also for the Electronic Ground Support Equipment (EGSE), and are specifying use of 1355 to their subcontractors.

At the other extreme, 4Links is jointly with Keele University presenting a paper at EMMSEC 97 which builds on the similarity between 1355 and a UART to suggest combining the two for a multimedia home network, with the potential of moving towards 1000 devices in approaching 1000 000 000 homes.

Between these two extremes, 1355 is being used in a variety of communications equipments, particularly for building switches for ATM, SCI, or FibreChannel, and there is considerable interest towards using it as a replacement for ATM switches in IP (Internet Protocol) switches. Its low latency and scaleable system throughput make it attractive for Networks of Workstations (NoWs). While it is not yet used for embedded fault-tolerance, cars and machinery are being designed where some of the function is taken away from the driver or operator, so a network is required which continues to operate even if a link becomes disconnected or one of the processors goes faulty, and 1355 is one of the few candidates which come near to meeting these requirements. The communication model used by 1355 is particularly appropriate for distributed systems running the JavaPP secure Plug and Play derivative of Java which combines Java with the formal basis of Communicating Sequential Processes (CSP).

1.3.3 Market forecasts

The **Space** market will take a few hundred boards, and positive experience of the use of 1355 will cause it to be used by the contractors in other industrial applications, leading over a few years to sales of thousands of boards. By being first to market, 4Links can expect a substantial share of this market.

The market for **home networks** has yet to be established, and has long been waiting for both technology and applications. The coming together of computers and TV, together with voice recognition and intuitive interfaces such as WWW browsers, suggest that both technology and applications are becoming ready. The potential market of anything up to a TeraDevice (a million million chips, or 100 billion ECU even at a low price of 0.1 ECU per chip), will be hotly contested. But the qualities of 1355, demonstrated by this project, will make this European technology a strong candidate for the market.

The market for **IP switches** is at its infancy, but with the massive growth in Internet, there will probably be even more massive growth in IP switches, to the extent of sales of hundreds of boards for development followed by hundreds of thousand if not millions of chips. Companies in Europe, USA. and Canada are planning to use 1355 for these products and are potential customers for both boards and chips.

A number of companies are using 1355 to build **switches for ATM, SCI, and FibreChannel**. Generally they propose to hide 1355 within the switch box, but some are appreciating the reduced cost of the ports of an "ATM" switch if the 1355 links are brought out as native ports. Even for development, this market could use hundreds of boards and thousands of chips.

For optimised **JAVA communications**, the market growth rate is so huge, that integrated chips will be needed and will sell in many millions. Here, the ARM as the preferred processor for the

Network Computer, is ideally combined with the circuits demonstrated on this project. Although the integration is preferred, it is possible that a \$3 chip for a 1355 port such as this project will demonstrate would be very attractive for this market and could itself sell in tens of millions.

Initial interest in 1355 has been expressed by the EBU for use in **TV studio equipment**. The precursor to 1355 (OS links of early transputers) has a long history of being used in studio equipment, for example by Quantel and in the Trilogy Commander. As with Space, the market is not for huge volumes, but it can use thousands of boards and many tens of thousands of chips.

Many of the applications of 1355 are currently limited either by the performance of the existing board products or by the withdrawal of key components on the boards they use. Possible customers for a faster board with assured component supply, and who need the full benefits of 1355 not available to them from their existing boards, are listed against the applications below. Several of these customers need only to port the applications, which should lead to more rapid sales take-up than if they had to develop the applications from scratch.

- Network of workstations (NoW) (Parsys, Parsytec, Alpha Data)
- Embedded fault-tolerance (Eonic, CERN, DSS)
- Drivers for Windows NT and/or 95 (PACT, DSS, ELCOM)
- TCP/IP, possibly with Windows driver (PACT, Surrey U)
- JavaPP, using a class to drive the board directly (Twente U, Kent U, Bristol U)
- Database system (Napier U, Parsys)
- Multimedia network to prototype a home network (Keele U, PACT)

1.3.4 Potential impact on Industry and Society

For industry, and particularly for the low-volume users of 1355, SOHI offers a product which they can buy and use. For the high volume users, SOHI offers a means of developing the applications and of proving the design of the logic and software used on the demonstrator board.

For society, the potential impact of a single interface which is used for any connections between anything containing microprocessors is huge. A useful analogy is with World-Class Manufacturing, which has completely changed the face of manufacturing industry over the last 50 years. The emphasis on Just-In-Time, Flexible Manufacturing, Zero Defects, Zero Waste, Minimal WiP, Minimal Delay, Minimal Batch-size, all have strong analogies with 1355, as shown in the table in Appendix A. Many of the competing technologies are analogous to manufacturing of the 50s or early 70s. Of course the transition to current World-Class Manufacturing took many years, and the engineers of the 50s were not ready for all the changes at once.

The change towards pervasive use of 1355 may not have quite the same impact as World-Class-Manufacturing, and it will only happen if 1355 products are available and can be seen to perform. SOHI demonstrates both availability and performance.

1.3.5 Needs and opportunities

In fact, the needs of networks for moving data around to produce an end-result are very similar to the needs in manufacturing for moving raw materials and components around to produce manufactured product. Minimal delay requires small buffers and small buffers require and give fast response. Flexible encapsulation of other protocols means that the same network can be used for a variety of other protocols, with negligible change-over time between them. A broken machine or pallet might cause a short gap in production for a small proportion of the factory, but there should be parallel machines and paths that are not delayed at all, and the fault should be removed from being a bottleneck very quickly. So the need for characteristics of 1355 is fairly universal.

The need for the SOHI development is to show the full benefits of 1355 without dependence on components which have bugs and are liable to be withdrawn.

The opportunity is a substantial market for the boards produced for demonstration, and the possibility of a much larger market for chips and the IPR embodied in the design of the board.

1.3.6 Analysis of foreseen competition

The major competition is from the serial interface technologies such as ATM and 1394, which have better market share and all of which have serious shortcomings. But even with these technologies seen as competitors, they can also be seen as complementary to 1355, and indeed as a market for 1355 to provide inexpensive switching technology inside ATM products.

From within 1355, the existing board products based on SGS-THOMSON components need to be replaced. 4Links would welcome competition from other board manufacturers of boards using alternative 1355 technology sources. These may include the CW-1355-C111 link macrocell in PLD from 4Links, or any alternative macrocell, or the SMCS chip from DSS/Temic/MHS resulting from the DIPSAPP project. There is indeed some motivation for using the SMCS chip on this project, as Virtuoso has been used with this chip and with a host connection via 4Links existing PCI board. But it is important to demonstrate the hardware routing capability of 1355, which is more easily done with logic implementation in PLD and FPGA, and for an SME it is a much better demonstration of best practice to convert from FPGA to a small ASIC rather than to one of the size of SMCS.

1.4 European dimension

Europe benefits from greatly improved exploitation of the excellent technology developed under a variety of European projects, but which the original technology developer has failed to exploit.

Projects under which the 1355 standard was developed include the Heterogeneous InterConnect (HIC) ESPRIT project, with further development and applications under Macramé and Arches. Together with part funding on the earlier PUMA and GPMIMD projects, a total probably exceeding 50MECU has been invested in the technology by companies and by the European Commission. Some of this has been invested by SGS-THOMSON, who have subsequently decided to withdraw the chips which implement the technology and on which all the other investors in the technology depend.

For the particular application of spacecraft the DIPSAPP2 project provides alternative interface chips, but does not provide the hardware routing capability which SOHI demonstrates.

So SOHI is a very small investment, mainly to demonstrate best practice from an SME, but which goes a very considerable way to plugging the gap made by SGS-THOMSON's withdrawal of 1355 components, and to provide the EC and others who have substantially invested in the technology with an alternative source of components.

To plug the gap in marketing and publicising the technology, and before they withdrew the components, SGS-THOMSON encouraged the formation of the 1355 Association. Members of the 1355 Association come from most European countries, with the seven officers of the Association coming from six European countries. Many of the potential customers for boards and for chips are in Europe, but there are also potential customers in Canada, USA, and Japan.

The proprietor of 4Links is editor to the 1355 Association, and in that capacity has commissioned eight papers for two sessions of the EMMSEC 97 conference, and has edited the contents of the Association's web site, with material from most of Europe.

The SOHI project will use ARM, a European processor, and Virtuoso, a European Real-time Operating System.

WP 1.3	PCB commissioning
Need	To prove the functionality of the prototype printed circuit boards
Objectives	To provide boards for software development that are free from hardware bugs
Who	4Links
Approach	<p>The links and routing switch will be tested independently by connecting them to each other and to an existing 4Links PCI board.</p> <p>The ARM will be tested by running ARM test programs as provided for the development board</p> <p>The PCI interface will be tested initially by reading and writing RAM, with the links and ARM disabled.</p> <p>Integration will be tested with small test programs, the writing of which may be small subcontracts either to Keele or to an independent software consultant.</p>
Milestones	<p>Isolated tests of links, ARM, and PCI month 5</p> <p>Demonstration of integrated functionality month 6</p>
Deliverables	Report on PCB and logic development, functionality, and design methodology month 7

WP 2.1	Host Interface software development
Need	Software to drive the board from the PC's hardware, at least under DOS
Objectives	To provide an interface for messages and virtual channels with a reasonable throughput and latency, targeted at 20 to 40 Mbytes/s on long messages (64 bytes or more) and latency limited by the Operating System rather than by the hardware or software interface.
Who	Subcontract to Keele University and to Eonic
Approach	Keele have developed a simple host interface for the 4Links PCI-1355 board, and Eonic have also developed a host interface for the board to connect to Virtuoso. The use of different PCI hardware, and particularly the use of master mode accesses to PCI, will require minor changes to this software. These changes will be done initially by Keele and then integrated with Eonic's host interface.
Milestones	<p>Basic functionality of PCI host interface month 7</p> <p>Functionality with target performance month 9</p>
Deliverables	Report on functionality and performance of host interface software month 10

WP 2.2	Porting Virtuoso to board
Need	Software is needed to manage the communications and routing switch, and to hide the latency of PC operating systems at least at the level of packets, so that the PC only sees messages. These functions are provided by Virtuoso, and so we need to run Virtuoso on the ARM processor on the board
Objectives	To run Virtuoso on the board, so that it communicates both with the host PC and with the links.
Who	Subcontract to Keele University and to Eonic
Approach	The porting will be done jointly by Keele, who have knowledge of the board, and by Eonic, who have knowledge of Virtuoso.. The initial port will use Virtuoso's programmed through-routing, rather than the hardware routing provided by the routing switch.
Milestones	Small network built with three or so boards each communicating under Virtuoso month 12
Deliverables	none

WP 2.3	Modifications to Virtuoso to handle the hardware routing switch
Need	In a Virtuoso network, any port can be connected to any other port, and if there is not a direct path between two nodes, Virtuoso connects them by a virtual path by programmed store-and-forward routing through intermediate nodes. This approach can be used for 1355, but the very simple hardware routing protocols of 1355, which provide worm-hole/cut-through routing, offer substantial improvement in both throughput and delay compared with programmed through routing via processors. So by enabling Virtuoso to handle the hardware through-routing, its functionality is unchanged, but the network performance is substantially improved.
Objectives	To modify Virtuoso to construct and respond to packet headers appropriate for hardware routing.
Who	Subcontract to Eonic
Approach	The packet structure of 1355 is very similar to the packet structure of Virtuoso, so the main part of the change is probably understanding just how similar they are and where there are subtle differences. It is proposed that this work on understanding be carried out ahead of the availability of prototype PCBs, and so before the work on the host interface and on porting Virtuoso to the board is carried out. Once the host interface and port have been completed, the hardware and other software will be used to develop and prove the changes required for hardware routing.
Milestones	Changes understood and specified month 5 Changes programmed and commissioned on the boards month 13
Deliverables	Report on software development including performance comparison between hardware and software routing month 14

WP 5	Exploitation
Need	To gain maximum and earliest exploitation from the work on the project
Who	4Links
Objectives	<p>To promote the IEEE 1355 standard through demonstration of the prototype board, the small ASIC chips, and the board using these chips.</p> <p>To increase sales of 4Links board products</p> <p>To increase sales of programmed PLD and FPGA chips and IPR of the C111 link macrocell, of a low-valency routing switch, of a 32-bit wide interface to 1355, and of a logic combination of all of these.</p> <p>To prove the combination of ARM plus 1355 to the extent that it is possible to construct a business plan for the development of a single chip integrating ARM processor plus 1355 links.</p> <p>To prove the combination of Virtuoso + 1355 hardware routing in terms both of performance and to give Eonic a platform for developing products for the market for embedded fault-tolerance.</p>
Approach	<p>Preliminary data sheets will be produced for the board, for the logic elements, and for the chip. These preliminary data sheets will be sent out by mailshot and email and advertised on the Web.</p> <p>4Links will be exhibiting at EMMSEC 97 and if the project is approved by then will use the exhibition as an opportunity to promote the project.</p> <p>The project will present as complete results as possible to EMMSEC 98, and will be present at least one other trade show or conference between EMMSEC 97 and EMMSEC 98. At least one further trade show will be used to present the full results and demonstrations.</p> <p>The final project report will be sent as widely through Europe as possible.</p>
Deliverables	<p>Publicity material and conference papers as produced throughout the project months 1-18</p> <p>First draft of business plan for combined ARM/1355 chip development month 9</p>

WP 6	Management
Need	Management of the project and producing the required reports.
Who	4Links
Objectives	To ensure the project either runs to plan, or if change to plan is needed, to provide timely response to the need for change.
Approach	A considerable proportion of the project work will be subcontracted. Although the subcontractors are organisations and people that 4Links has worked with before, the subcontract relationship still needs to be managed. The management work package of the project will continue one month beyond the end of the project, in order to produce a final project report
Deliverables	Project progress reports months 6, 12 Final report month 19

The tables below summarise the milestones and deliverables listed in the above tables

WP 1.1	M 1.1.1	PCB Layout complete	month 2
	M 1.1.2	Assembled PCBs received	month 3
WP 1.2	M 1.2.1	Logic design complete	month 3
WP 1.3	M 1.3.1	Isolated tests of links, ARM, and PCI	month 5
	M 1.3.2	Demonstration of integrated functionality	month 6
WP 2.1	M 2.1.1	Basic functionality of PCI host interface	month 7
	M 2.1.2	Functionality with target performance	month 9
WP 2.2	M 2.2.1	Small network built with three or so boards each communicating under Virtuoso	month 12
WP 2.3	M 2.3.1	Changes understood and specified	month 5
	M 2.3.2	Changes programmed and commissioned on the boards	month 13
WP 3	M 3.1	Design port complete	month 14
	M 3.2	Order for chips accepted by ASIC house	month 15 (mid)
	M 3.3	Chips delivered	month 17
WP 4	M 4.1	PCB Layout complete	month 16
	M 4.2	Assembled PCBs received	month 17
	M 4.3	PCBs tested and working in network of at least five boards, with the software developed in the project	month 18

WP 1.1	D 1.1.1	Specification of hardware, and of the software interfaces of the hardware month 1
WP 1.3	D 1.3.1	Report on PCB and logic development, functionality, and design methodology month 7
WP 2.1	D 2.1.1	Report on functionality and performance of host interface software month 10
WP 2.3	D 2.3.1	Report on software development including performance comparison between hardware and software routing month 14
WP 3	D 3.1	Preliminary Data Sheet for chips month 13
	D 3.2	Report on conversion process month 18
WP 4	D 4.1	User manual for the board month 17
	D 4.2	Glossy data sheet for board, including photo showing the new chips and ARM month 18
WP 5	D 5.1	Publicity material and conference papers as produced throughout the project months 1-18
	D 5.2	First draft of business plan for combined ARM/1355 chip development month 9
WP 6	D 6.1	Project progress reports months 6, 12
	D 6.2	Final report month 19

1.6 Exploitation plan

The exploitation plan is built into the complete SOHI proposal and the choice of processor and RtOS.

The design of a new PCI board, incorporating feedback from customers about the existing 4Links PCI-1355 board further establishes 4Links as a responsive supplier of useful board products to users of 1355, and makes it easier for those customers to exploit their use of the 1355 standard. Sales of the prototype board, before integration of the 1355 macrocell, are likely to be in the tens to small hundreds. With the lower costs possible from integrating the 1355 macrocell onto a small ASIC, sales of the revised board could run to several thousand, even from the customers identified as already having applications of 1355, and in turn from their customers.

Similarly, use of the logic macrocell design of the 4Links CW-1355-C111 establishes further confidence in the design and strengthens 4Links ability to sell both programmed PLDs and IPR. This will be developed further by offering the designs of the low-valency router and 32-bit-wide interface both as programmed PLDs/FPGAs, and as IPR.

The small hardware router itself will be designed using protocols invented jointly by Keele and 4Links for which 4Links has applied for a patent, and so the routing function offers further opportunity for exploiting the invented technology. 4Links and Keele have an agreement in place concerning IPR resulting from collaboration. This IPR also opens up additional opportunities for consultancy in specific developments of 1355.

Proving the conversion of the PLD design to ASIC silicon gives customers much more confidence in this design than if they were to be the first customer to take it to silicon, so should generate sales of the macrocell as well as sales of chips. If the target chip cost of \$3 is achieved, it should be possible to break-even on chip sales of around 2,500 while potential sales, as described in the above section on markets, are many times this quantity.

Many users of 1355 would prefer the links to be integrated with a processor. In choosing a processor, one is needed which is available as a core macrocell, which is available from a wide variety of sources for a wide variety of applications, which is heavily used in embedded applications, and which is regularly updated to the latest silicon process technology. On all counts ARM meets these needs, and initial informal contact with ARM has suggested an interest in developing a chip which integrates ARM and 1355. Clearly such a development would be at less risk, both commercially and technically, if the combination was shown to work as a PCB and small ASIC first. Part of the exploitation, therefore, of the SOHI project, will include the first draft of a business plan for the development funding for such a chip.

In constructing and editing the 1355 Association's web site, 4Links has produced a wide range of tutorial and technical information about the 1355 standard. This experience will be used in the generation of web-accessible sales and promotional material both for the project and for the resulting technology.

Similarly as 4Links was the only exhibitor of 1355 technology at EMSYS 96, will exhibit at EMMSEC 97 and has co-ordinated the 1355 Association's exhibit at EMMSEC 97, 4Links will continue to have presence at useful conferences and trade shows. As well as EMMSEC 98, at least one other trade show or conference will be used between EMMSEC 97 and 98, and at least one will be used later to show the results of the project. In addition, Eonic Systems have an excellent record of publicising their work with newsletters and trade shows, and their publicity will further increase the exposure of the results of the project.

1.7 Project management

A substantial proportion of the SOHI project is subcontracted to others who would, on a larger project, be partners. But a project with total labour content of little over one man-year, spread between several partners, would give these organisations unnecessary overhead. 4Links has experience of managing subcontract development, and will therefore assume the role of Co-ordinator and Project Manager.

Management and exploitation will be done by 4Links, together with PCB design, layout, and co-ordination of manufacture. Logic design will be subcontracted to Keele. Porting Virtuoso to the board will be done jointly by Keele and Eonic. The changes to Virtuoso to handle hardware routing will be subcontracted to Eonic. Conversion from CPLD/FPGA to small ASIC will be done jointly by 4Links and Keele, with the final PCB done by 4Links

The primary means of co-ordinating with the subcontractors and making decisions is by regular phone and email contact, supported by monthly meetings when there is significant activity required of the subcontractor. Disputes are not expected, but if they do arise, they will be resolved by meeting, if necessary at an additional meeting to the monthly meetings.

While publicity material will be made available on a publicly accessible web site, private material to the project will be held on an unpublicised web site, with access control or encryption of any confidential or proprietary material. This private site will be used as a document archive of the latest issued versions of both designs and documents, so that there is an archive independent of any of the participants in the project.

1.7.1 Relations and dependencies on other projects

The SOHI project is closely related to a number of other EU projects, but its structure allows it to succeed or fail on its own merits independently of these other projects. Indeed the choice of an established processor and established RtOS, and the decision to avoid using existing and threatened 1355 chips, ensures this independence. Several applications of 1355 being developed in other EU projects are suffering from withdrawn components or from poor performance of existing 1355 boards. So the success of SOHI will have a positive effect both on the Arches and DIPSAPP2 projects, and on any project involving the 1355 Association.

1.8 The Proposer

The proposer is 4Links, which offers boards, chips, IPR, and consultancy for links, with particular emphasis on the DS-SE and DS-DE versions of IEEE 1355/HIC links.

4Links products include the PCI-1355 board, which provides a simple interface from the PC to 1355, with limited performance but significantly higher performance than alternative ISA board products. A recent additional board is the IDE-1355, which provides an interface between two low-cost IDE disk drives and a 1355 link. This board will be used for database system development for a data mining application. 4Links also sells the CW-1355-C111 link macrocell, both as programmed PLD and as IPR either as JEDEC programming file or as logic equations or VHDL for use in the customers' own designs. The experience gained from these products equips 4Links also to offer consultancy to anyone needing help with 1355 or with similar communications technology.

4Links has worked closely with Dr B M Cook of Keele University, who helped with the design of the PCI-1355 board and who, after discussion with 4Links, designed the logic for the IDE-1355 board and the CW-1355-C111 chip, making these commercially available through 4Links. Dr Cook has also, jointly with 4Links, invented developments from 1355, for which patents have been applied for by 4Links under an agreement between Keele and 4Links.

1.8.1 Profile of Paul Walker, Proprietor of 4Links

Paul Walker registered a consultancy business for VAT in 1993 and changed the business name to "4Links for technical help" in 1995. He has provided consultancy in design and in communications and computer electronics, but has exploited his technical experience most effectively in specialising in the IEEE 1355 standard. He has been evaluator and reviewer for ESPRIT projects and evaluator for UK EPSRC projects. He is named in about 10 patents applications, most of which have now been granted, and in areas covering communications, memory, fault-tolerance and packaging. He is editor to the 1355 Association. He is a non-executive director of IC Routing Ltd and of the 1355 Association Executive Ltd. He has published many papers and technical articles, mostly concerning IEEE 1355, communications, or transputers, but also including one on the analogies between communications and modern production techniques.

While at INMOS, from 1979 to 1993, he produced the early documentation on the transputer and its applications and put this into effect by managing the INMOS board products group. During this time the group originated the TRAM family of transputer modules, which became an industry standard and were widely acclaimed for their simplicity and ease of use.

While managing the INMOS board business, a variety of subcontractors were used for both design and manufacture, and the turnover achieved by the small group never exceeding 12 people, most of whom were newly graduated from University, approached \$1M per month. Turnover per employee of this young group was around \$700k.

As 4Links, Paul Walker has contributed as subcontractor to both Macramé and Arches projects which are developing and demonstrating applications of 1355. While at IMNOS contributed to the PUMA, GPMIMD and HIC projects, all of which contributed to the definition and development of the link technology which became IEEE 1355.

The proprietor of 4Links is a member, and past chairman, of the IEE's Professional Group M1 for Design and Development. This arose from and increased his interest in best practice in design, and in the use of the "House of Quality" techniques.

The external expenditure is summarised in the table here, with more detail following the table.

WP	What	Cost, kECU
1.1,5	PCBs	4
1.1,5	Components for PCBs	8
1.1,5	PCB Assembly	4
1.2	CAD for PCB	1.5
1.2	CAD for FPGAs	15
1.2	Soft macrocell for PCI in FPGA	8
2.1	ARM devt. S/W	4
4	FPGA Conversion to small ASIC	22
5	Publicity Material + web site	3
5	Travel etc. for exploitation	5
6	Travel for management	5
Total		79.5

The PCB cost is for two versions of the PCB design, one for prototypes, the other for the small ASIC chips, with the expectation of building ten prototypes and 20 boards for the chips. Cost including tooling for a batch of ten boards is around 1.5kECU, for 20 boards around 2.5kECU.

The components for the PCBs include some expensive FPGAs, as well as the ARM processor chips. The boards with the small ASIC chips will have significantly lower component cost than the prototype boards, but the PCI interface still needs an FPGA at 120 ECU each, and 8kECU is a reasonable overall estimate for the total component costs for the project.

PCB assembly for these early low volumes will be subcontracted and done by hand. While the rate is very reasonable at about 35ECU per hour, each board is 3 to 4 hours assembly, which leads to a total assembly cost of about 4kECU.

CAD for FPGA development is expensive, and 4Links has chosen the devices in the past on the basis of those which have development tools costing \$100 or so. The capability that can be bought for \$15k to \$20k is not as great as would be ideal, but satisfactory FPGA tools can be bought for this price, and so the estimate of 15kECU is a reasonable compromise between cost and capability.

4Links existing PCI board uses an off the shelf PCI chip, because the FPGA implementations at the time were unstable, and the FPGAs in which they fitted were extremely expensive. This situation has since greatly improved. Given the desire to move towards integration in ASICs of the 1355 logic designs, an FPGA implementation of the PCI interface is a timely move. The 8kECU price is based on both Xilinx and Lucent offering the master mode interface design for \$10k.

ARM offer a range of development software and hardware development boards, at reasonable prices. The 4kECU should be adequate for development and debugging of simple test software for commissioning the board.

The cost of FPGA conversion to ASIC has been reducing, and 4Links has a quote for a 2000 gate conversion at \$10k NRE plus a unit cost per device for 1000 devices of less than \$2. An alternative quote, is for \$25k, with the quantity of devices supplied depending on the work required in the conversion, and on the size of the chip. The 2000 gate quote is sufficiently reasonable that it would be worth-while to put more functionality in the device, perhaps to reduce the external circuitry required to buffer external cables. The logic for the 1355 port can be used directly to build the 4-port routing switch required in the SOHI project, but a scaleable switch of more than 8 ports requires a small amount of extra logic which has already been designed and which may be worth including. The House of Quality technique will be used to establish the customer value of these additional features, but it seems sensible to use the higher \$25k quotation as the basis of the 22kECU requested for the FPGA conversion.

The 3kECU for web site and for publicity material is about 1k for commercial web space and 1k each for printing two publicity leaflets, one early in the project and the other to describe the chips and report project results later in the project.

Exploitation travel includes three conferences or trade shows, at around 1600 ECU per conference.

Management travel includes seven meetings with Eonic in Belgium, at about 500 ECU per meeting, plus 10 meetings with Keele at about 150 ECU per meeting

Appendix A

This analogy is presented as an appendix as it is not directly in support of the proposal. The Specific Information Document for small demonstrator proposals does, however, ask for the impact on industry and society. While no claim can be made that 1355 will have quite the same impact on industry and society as the paradigm shift to modern manufacturing methods, the closeness of the analogy strongly suggests that a very major impact is waiting to be made from communications which model the improvements in manufacturing.

Old production line	Modern manufacturing	IEEE 1355
Bottlenecks	Spare or flexible capacity to eliminate bottlenecks	Multiple paths and adaptive routing to eliminate bottlenecks, provide fault tolerance
Rigid production lines	Flexible manufacturing	Flexible encapsulation of other protocols, flexible network topologies
Quality doesn't matter/repair if faulty	Quality is paramount, Zero defects	Reliable links, buffers never overflow
Don't change it	Continuous improvement	Adding nodes and links continuously improves the network
Lead time is irrelevant	Just-In-Time because delay reduces quality, reduces customer service, and reduces throughput	Worm-hole routing and flow-control minimise delay
Long conveyor belt	Many small, independent, cells	Many independent links
Large batch sizes	Small batches, in trays, preferably one unit per tray	Small packets, appropriate for the application
"Push" components onto the line	When a tray is used, the tray goes back as an order to "pull" more components	Feedback flow-control "pulls" data when there is space for it
Long change-over time	Very fast tool-change	Fast, widely distributed, independent, arbitrations; fast changeover between different packets and protocols
Environment does not matter	Waste of any kind is damaging to the environment (as well as profit)	Eliminate wasted data from buffer overflow, eliminate wasted power driving unnecessary wires, eliminate unnecessary RF pollution
Inventory is asset	Inventory is liability	Minimise data buffers
Make 50% profit margin once per year	Make 20% profit margin 10 times per year	1/5th the link speed in a switched network can offer 20 times the overall throughput of the bus

Table A: Analogies between IEEE 1355 and the recently shifted paradigms in manufacturing