

# 4L-C112-XL



100 Mbit/s Asynchronous Receiver/Transmitter (ART)

Licence for design targeted to Xilinx FPGA

## Product Outline

The 4L-C112-XL is like a UART, with the FIFOs and automatic flow-control of the latest UARTs, but ten or more times as fast as the fastest UARTs. Extra functions, not found in standard UARTs, include hardware autobaud, a simple packet protocol, and hot-plug support.

All this function fits the smallest Xilinx FPGA, and runs at 100 Mbaud full-duplex on the slowest available (and hence lowest-cost) version of this FPGA (claimed by Xilinx to be \$2.95 in Q4-1998).

An FPGA programmed to be a 4L-C112 is just as universal as a UART, but the term UART is strongly identified with RS232, and the protocols of the 4L-C112 are those of the IEEE standard 1355-1995. The device is most certainly an Asynchronous Receiver/Transmitter, and so it goes under the acronym **ART**.

The 4L-C112-XL is a Licence to the design for Xilinx FPGA, for either source or binaries.

## Features

- ✧ Autobaud on incoming serial data between 2 Mbits/s and 100 Mbits/s.
- ✧ Clock recovery from incoming serial data, permits spread-spectrum Tx Clock
- ✧ 16-byte deep FIFOs on both Transmit and Receive.
- ✧ Cascadable, handshaken, byte-wide (8+1 bit) FIFO port interfaces.
- ✧ Autonomous flow-control so that FIFOs never overflow.
- ✧ Accepts arbitrarily long or short packets.
- ✧ Hot-Plug support with detection of unplug or no input, autonomous restart on plug-in.
- ✧ Improved initialisation compared with previous 1355 implementations.
- ✧ Targeted to the smallest Xilinx 4000E series and Spartan FPGAs.

## Character alphabet

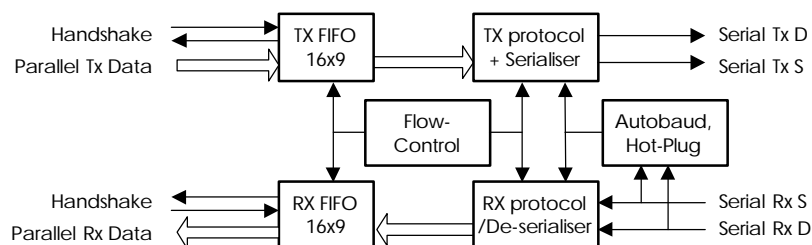
Characters transmitted transparently through FIFOs and serial link:

- Data** Data values 0 to 255
- EOP1** End of Packet
- EOP2** Exceptional End of Packet, may indicate possible corruption of packet

Characters local to a serial link, not passed through FIFOs:

- NUL** Padding when there is no data to send, or insufficient credit from far end
- FCC** Flow-control character, gives transmitter credit to send eight more characters

## 4L-C112 Block Diagram



The 4L-C112-XL has been developed in collaboration with Dr B M Cook of Keele University

\* Use of a spread-spectrum transmit clock is patent pending to 4Links.

Xilinx' trademark of the name Xilinx is acknowledged

The information supplied in this Product Outline is believed to be accurate. 4Links reserves the right to change specifications or to discontinue products without notice. 4Links assumes no liability arising out of the application or use of any information or product, nor does it convey any licence under its patent rights or the rights of others.