

# CW 1355 C111

## IEEE 1355-1995 Interface

### Features

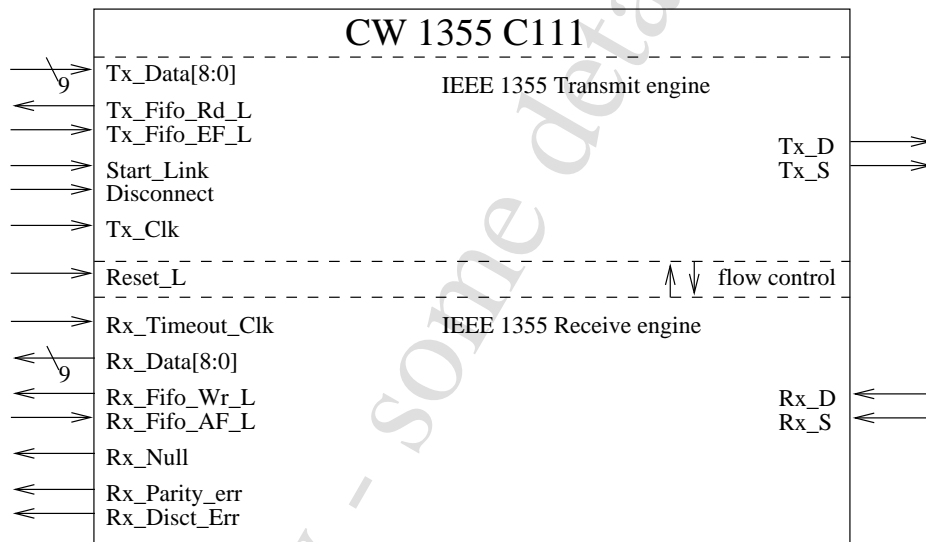
- Low cost, 44-pin PLCC
- High speed data transmission up to 100Mb/s
- May be used with a spread-spectrum clock to reduce EMI
- Simple byte-wide interface to FIFO buffers
- Uses standard off-the-shelf programmable logic
- Programming data available under licence

### Description

The CW 1355 C111 is a stand-alone integrated circuit providing an interface to an IEEE 1355 link. This implements a simple communication standard at up to 100Mbit/s with a straightforward low-level connection using Data/Strobe encoding at TTL levels. Buffering into a differential signal enables 100Mb/s communication over tens of metres using low-cost twisted pair cable.

All low-level flow control and error detection is handled within the device, the user supplies and receives streams of data and packet-marker tokens. The interface is configured for direct connection to send and receive FIFO's, but the transmit FIFO need not be used and a direct interface for this is provided. Connection to computer busses and low cost microcontrollers is easy and allows IEEE 1355 communications in embedded applications.

### Functional Block Diagram



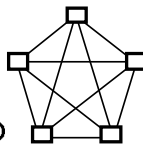
### For pricing and availability contact:

*Paul Walker*  
*paul@walker.demon.co.uk*  
*+44 1908 566253*

*4Links for technical help*  
*P O Box 816, Two Mile Ash*  
*Milton Keynes, MK8 8NS, UK*

*The CW 1355 C111 is a result of collaboration between 4Links and Keele University*

**4Links**  
for technical help



**KEELE**  
UNIVERSITY  
DEPARTMENT OF COMPUTER SCIENCE

Last revised: 8<sup>th</sup> November 1996

Signal	Pin	I/O	Description																																																		
Rx_D	31	I	Received data																																																		
Rx_S	32	I	Received strobe																																																		
Tx_D	37	O	Transmitted data																																																		
Tx_S	38	O	Transmitted strobe																																																		
Rx_Data[8]	30	O	Incoming data appears as a 9-bit word, the ninth bit ( <i>Rx_Data[8]</i> ) indicates how to interpret the remaining eight bits.																																																		
Rx_Data[7]	29	O																																																			
Rx_Data[6]	27	O																																																			
Rx_Data[5]	26	O																																																			
Rx_Data[4]	22	O																																																			
Rx_Data[3]	21	O																																																			
Rx_Data[2]	20	O																																																			
Rx_Data[1]	19	O																																																			
Rx_Data[0]	18	O																																																			
<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="9">Rx_Data</th> <th>Interpretation</th> </tr> <tr> <th>[8]</th> <th>[7]</th> <th>[6]</th> <th>[5]</th> <th>[4]</th> <th>[3]</th> <th>[2]</th> <th>[1]</th> <th>[0]</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>D<sub>7</sub></td> <td>D<sub>6</sub></td> <td>D<sub>5</sub></td> <td>D<sub>4</sub></td> <td>D<sub>3</sub></td> <td>D<sub>2</sub></td> <td>D<sub>1</sub></td> <td>D<sub>0</sub></td> <td>Data[7:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>EOP</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>EOM</td> </tr> </tbody> </table>				Rx_Data									Interpretation	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		0	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Data[7:0]	1	0	0	0	0	0	0	0	0	EOP	1	0	0	0	0	0	0	0	1	EOM
Rx_Data									Interpretation																																												
[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]																																													
0	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Data[7:0]																																												
1	0	0	0	0	0	0	0	0	EOP																																												
1	0	0	0	0	0	0	0	1	EOM																																												
Tx_Data[8]	40	I	Outgoing data is presented as a 9-bit word, the ninth bit ( <i>Tx_Data[8]</i> ) indicates how to interpret the remaining eight bits.																																																		
Tx_Data[7]	41	I																																																			
Tx_Data[6]	42	I																																																			
Tx_Data[5]	43	I																																																			
Tx_Data[4]	3	I																																																			
Tx_Data[3]	4	I																																																			
Tx_Data[2]	5	I																																																			
Tx_Data[1]	6	I																																																			
Tx_Data[0]	7	I																																																			
<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="9">Tx_Data</th> <th>Interpretation</th> </tr> <tr> <th>[8]</th> <th>[7]</th> <th>[6]</th> <th>[5]</th> <th>[4]</th> <th>[3]</th> <th>[2]</th> <th>[1]</th> <th>[0]</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>D<sub>7</sub></td> <td>D<sub>6</sub></td> <td>D<sub>5</sub></td> <td>D<sub>4</sub></td> <td>D<sub>3</sub></td> <td>D<sub>2</sub></td> <td>D<sub>1</sub></td> <td>D<sub>0</sub></td> <td>Data[7:0]</td> </tr> <tr> <td>1</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>0</td> <td>EOP</td> </tr> <tr> <td>1</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>x</td> <td>1</td> <td>EOM</td> </tr> </tbody> </table>				Tx_Data									Interpretation	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		0	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Data[7:0]	1	x	x	x	x	x	x	x	0	EOP	1	x	x	x	x	x	x	x	1	EOM
Tx_Data									Interpretation																																												
[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]																																													
0	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	Data[7:0]																																												
1	x	x	x	x	x	x	x	0	EOP																																												
1	x	x	x	x	x	x	x	1	EOM																																												
Rx_Fifo_Wr_L	25	O	Data is written to the receive FIFO when this output is low. This is low for 2-bit periods of the received data.																																																		
Rx_Fifo_AF_L	28	I	This input indicates that the receive FIFO is almost full, it must go low when there are less than 16 words available.																																																		
Tx_Fifo_Rd_L	44	O	Data is read from the transmit FIFO when this output is low. This is low for 2-bit periods of transmit clock ( <i>Tx_Clk</i> ).																																																		
Tx_Fifo_EF_L	39	I	A low-level on this pin indicates that the FIFO is empty. In other words, a high level indicates that the FIFO contains data to be sent.																																																		
Tx_Fifo_EF_H	9	I	A high-level on this pin indicates that the FIFO is empty. This is provided as an additional indicator that may be used to prevent data from the FIFO being used while it is being filled ready for a burst transmit.																																																		
Rx_Parity_Err	15	O	If, after a valid input has been seen, a parity error is detected in the data then the <i>Rx_Parity_Err</i> pin will go high and remain there until reset is asserted. <i>Rx_Fifo_Wr_L</i> will not be asserted if <i>Rx_Parity_Err</i> is high.																																																		
Rx_Disct_Err	17	O	If, after a valid input has been seen, data is not received for at least the timeout period (as determined by the <i>Rx_Timeout_Clk</i> ) then this line will go high and remain there until reset is asserted. <i>Rx_Fifo_Wr_L</i> will not be asserted if <i>Rx_Disct_Err</i> is high.																																																		

Signal	Pin	I/O	Description
Rx_Null	16	O	After reset is de-asserted the receiver searches for a valid incoming Null character. A running pattern match is performed so it is unimportant exactly when the receiver starts - it will synchronise with a transmitter. After a Null has been seen the <i>Rx_Null</i> output will go high and stay at that value (regardless of whether errors are seen) until reset is asserted. No data can be received, nor any notice taken of parity or disconnect errors until a valid Null has been received.
Start_Link	8	I	After reset, the link is idle and transmits nothing until it is started. A non-empty transmit FIFO, a received Null or a high level on this pin start the link transmitter. Connect this pin to Vcc for the chip to start transmitting immediately after Reset is de-asserted.
Stop_Link	9	I	A high level on this pin forces the link transmitter to stop and force a disconnect error to be seen at the other end of the link. If necessary, the link will first be started so that at least one character is sent before stopping.
Tx_Clk	11	I	This sets the transmission speed, the transmit bit rate is equal to the frequency supplied at this pin.
Rx_Timeout_Clk	10	I	Line disconnection is detected by monitoring incoming signals for activity. If no activity is seen in the period between successive rising edges of the <i>Rx_Timeout_Clk</i> a disconnect error is reported. IEEE 1355 requires a period of 850ns, requiring a 1.176MHz clock at this pin.
Reset_L	35	I	All activity and internal status is reset by a low-level signal on this input. After this pin goes high the receiver will be looking for a valid Null token and the transmitter will be do nothing until it is started.
Gnd	1	I	System ground, this pin supplies current to the chip
Gnd	23	I	System ground, this pin supplies current to the chip
Vcc	12	I	System power, this pin supplies current to the chip
Vcc	34	I	System power, this pin supplies current to the chip
HoldToVcc	13	I	Connect this pin to Vcc, this is a signal input
HoldToVcc	14	I	Connect this pin to Vcc, this is a signal input
HoldToVcc	33	I	Connect this pin to Vcc, this is a signal input
HoldToVcc	36	I	Connect this pin to Vcc, this is a signal input
HoldToGnd	2	I	Connect this pin to Gnd, this is a signal input
DoNotWire	24		Do not connect anything to this pin

## Absolute Maximum Ratings

Supply voltage, Vcc	-0.5 to +7.0V
Input applied voltage	-2.5 to Vcc+1.0V
Off-state output voltage applied	-2.5 to Vcc+1.0V
Storage temperature	-65 to 125°C
Case temperature with power applied	-55 to 125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## DC Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units	
Vcc	Supply voltage	Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	4.75	5.25	V
		Industrial $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.5	5.5	
V <sub>IL</sub>	Input low voltage	0.0	0.8	V	
V <sub>IH</sub>	Input high voltage	2.0	Vcc+1	V	

## Capacitance

The maximum input capacitance of any signal pin is 10pF, measured at Vcc = 5V, V<sub>IN</sub> = 2.0V, T<sub>A</sub> = 25°C and test frequency = 1.0MHz.

## Lifetime

This device is a pre-programmed logic device, the manufacturers state that the program defining the internal logic will be retained for at least 20 years.

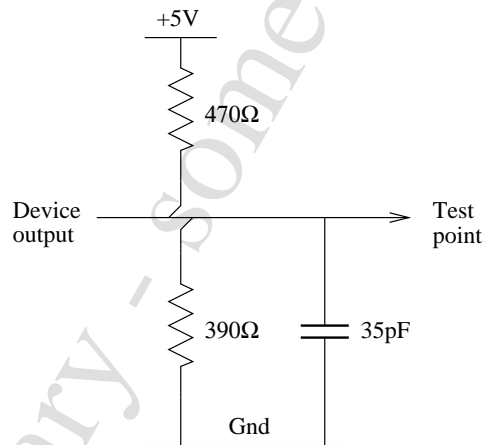
## DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OL}$	Output low voltage	$I_{OL} = 8\text{mA}$	-	-	0.4	V
$V_{OH}$	Output high voltage	$I_{OH} = -4\text{mA}$	2.4	-	-	V
$I_{IL}$	Input low current	$0\text{V} \leq V_{in} \leq V_{IL}(\text{max})$	-	-	-150	$\mu\text{A}$
$I_{IH}$	Input high current	$3.5\text{V} \leq V_{in} \leq V_{CC}$	-	-	10	$\mu\text{A}$
$I_{OS}$	Output s/c current	$V_{CC} = 5\text{V}, V_{out} = 0.5\text{V}$	-60	-	-200	mA
$I_{CC}$	Supply current	Industrial	-	TBD	TBD	mA
		Commercial	-	TBD	TBD	mA

## Switching Test Conditions

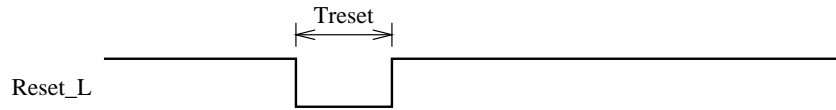
Input pulse levels	Gnd to 3.0V
Input rise and fall time	$\leq 3\text{ns}$ , 10% to 90%
Input timing reference levels	1.5V
Output timing reference levels	1.5V
Output load	see below

## Test load



Load capacitance includes test fixture and probe capacitance

## Timing Parameters - Reset



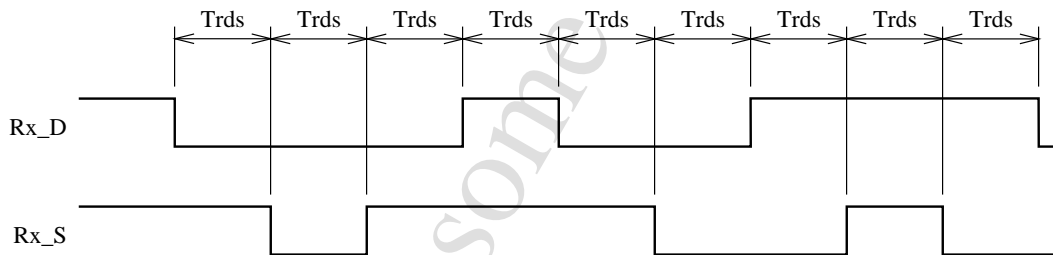
Parameter (see note)	Description	-50		-100		Units
		Min	Max	Min	Max	
Treset (1)	Minimum reset pulse width	15	-	10	-	ns

### Notes:

1. This pulse will reset the chip. Reset must be asserted for a much longer period to disable the transmitter for long enough to signal a line disconnect condition (set by the corresponding receiver's timeout period).

## Timing Parameters - Receive data from link

### Received data

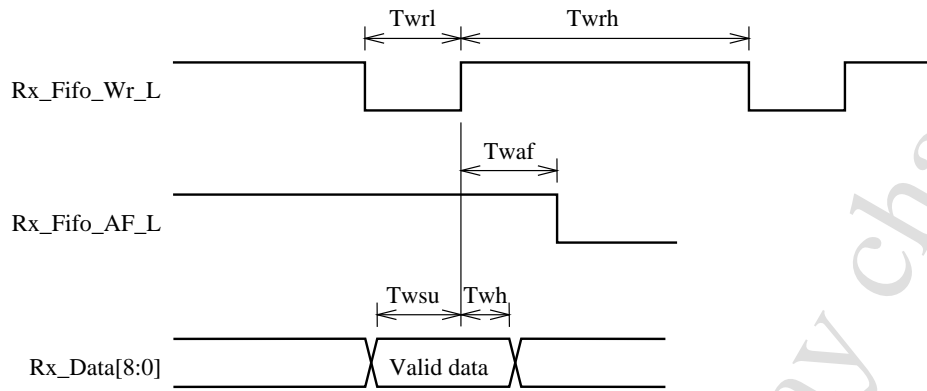


Parameter (see note)	Description	-50		-100		Units
		Min	Max	Min	Max	
Trds (1)	Data/strobe input edge separation	15	-	TBD	-	ns

### Notes:

1. The shortest permissible spacing between two consecutive edges on the data and strobe pins (one edge of either sense on each wire); this includes consecutive edges on either data or strobe.

## Write data to receive FIFO

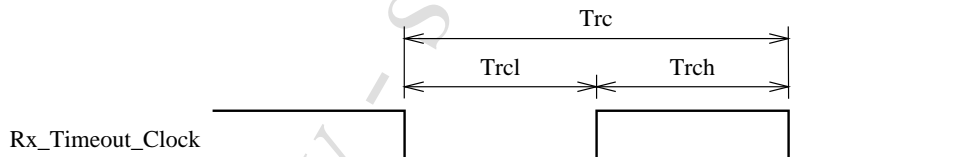


Parameter (see note)	Description	-50		-100		Units
		Min	Max	Min	Max	
Twrl (1)	Write pulse low time	38	-	18	-	ns
Twrh (1)	Write pulse high time	38	-	18	-	ns
Twaf	Read pulse to almost-full status	-	38	-	18	ns
Twsu (1)	Data valid before end of read pulse	38	-	18	-	ns
Twh (1)	Data valid after end of read pulse	38	-	18	-	ns

### Notes:

1. These times are 2ns less than the duration of 2 bits of received data, times given are at the maximum data rate.

## Receive timeout clock



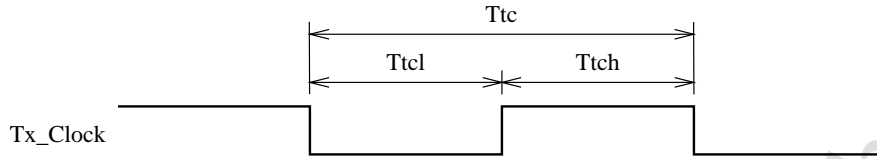
Parameter (see note)	Description	-50		-100		Units
		Min	Max	Min	Max	
Trcl	Receive timeout clock low time	6	-	4	-	ns
Trch	Receive timeout clock high time	6	-	4	-	ns
Trc (1)	Receive timeout clock total period	100	-	50	-	ns
Trf (1)	Receive timeout clock frequency, 1/Trc	-	10	-	20	MHz

### Notes:

1.  $Trc = Trcl + Trch$   
IEEE 1355 requires Trc to be 850ns, i.e.  $Trf = 1.176...MHz$ .

# Timing Parameters - Transmit data to link

## Transmit clock

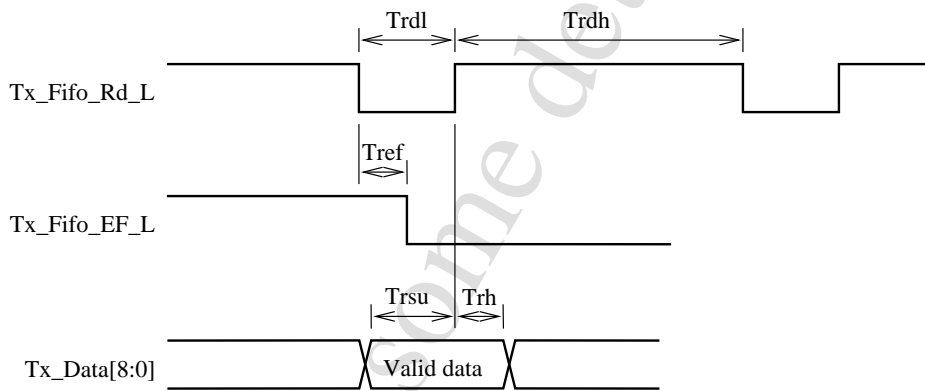


Parameter (see note)	Description	-50		-100		Units
		Min	Max	Min	Max	
Ttcl	Transmit timing clock low time	6	-	4	-	ns
Ttch	Transmit timing clock high time	6	-	4	-	ns
Ttc (1)	Transmit timing clock total period	20	-	10	-	ns
Ttf	Transmit clock frequency, 1/Ttc	-	50	-	100	MHz

Notes:

1.  $Ttc = Ttcl + Ttch$

## Read data from transmit FIFO

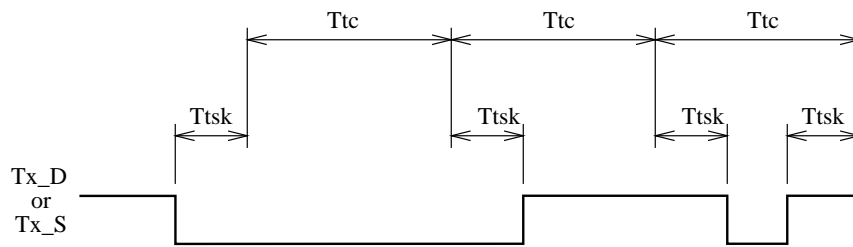


Parameter (see note)	Description	-50		-100		Units
		Min	Max	Min	Max	
Trdl (1)	Read pulse low time	118	-	58	-	ns
Trdh (1)	Read pulse high time	78	-	38	-	ns
Tref	Read pulse to empty status	-	TBD	-	TBD	ns
Trsu	Data valid before end of read pulse	12	-	TBD	-	ns
Trh	Data valid after end of read pulse	0	-	TBD	-	ns

Notes:

1. These times are 2ns less than the duration of 6 bits of transmitted data (i.e.  $(6 * Ttc) - 2ns$ ), times given are at the maximum data rate.
2. These times are 2ns less than the duration of 4 bits of transmitted data (i.e.  $(4 * Ttc) - 2ns$ ), times given are at the maximum data rate.

## Transmitted data



Parameter (see note)	Description	-50		-100		Units
		Min	Max	Min	Max	
Ttsk (1)	Data/strobe output skew	-	TBD	-	TBD	ns

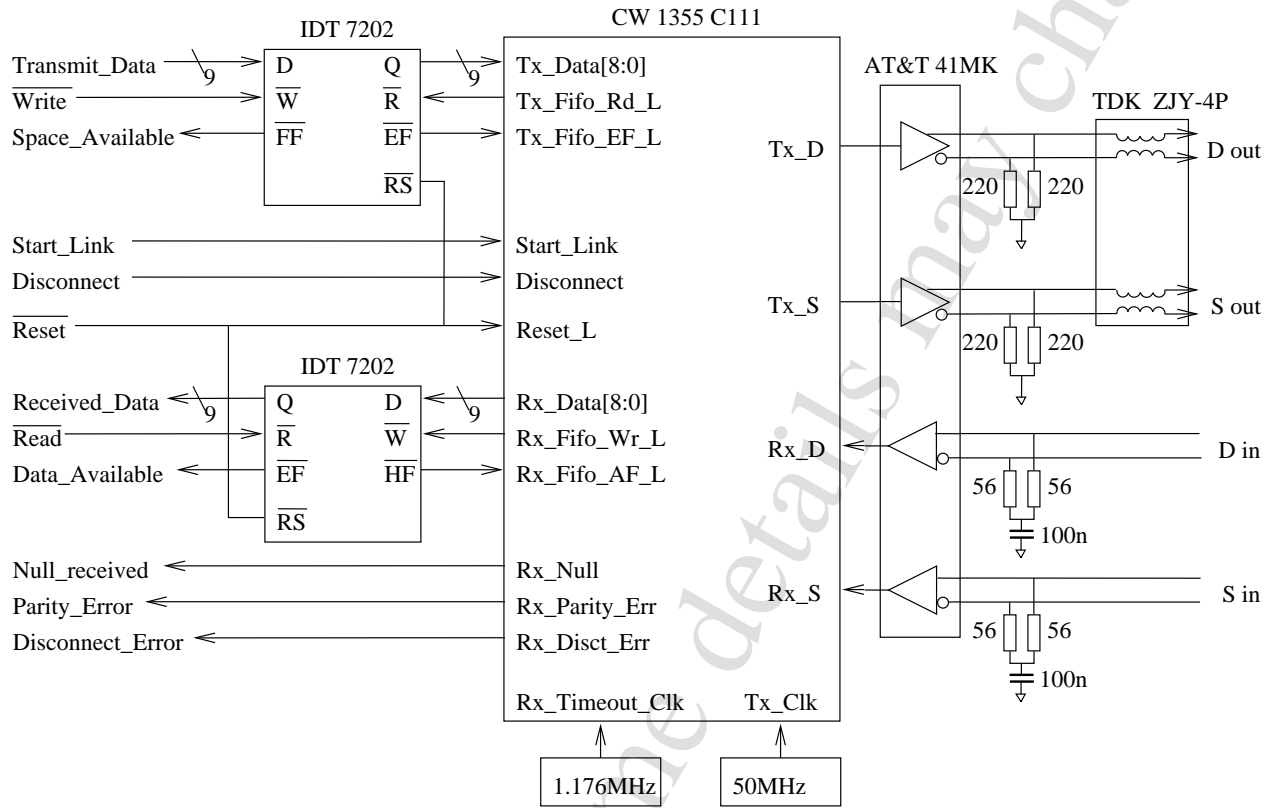
### Notes:

1. The maximum discrepancy between the time when a DS output edge (either sense) starts a transition and the theoretical ideal (i.e. all consecutive DS edges separated by  $Ttc$ ).

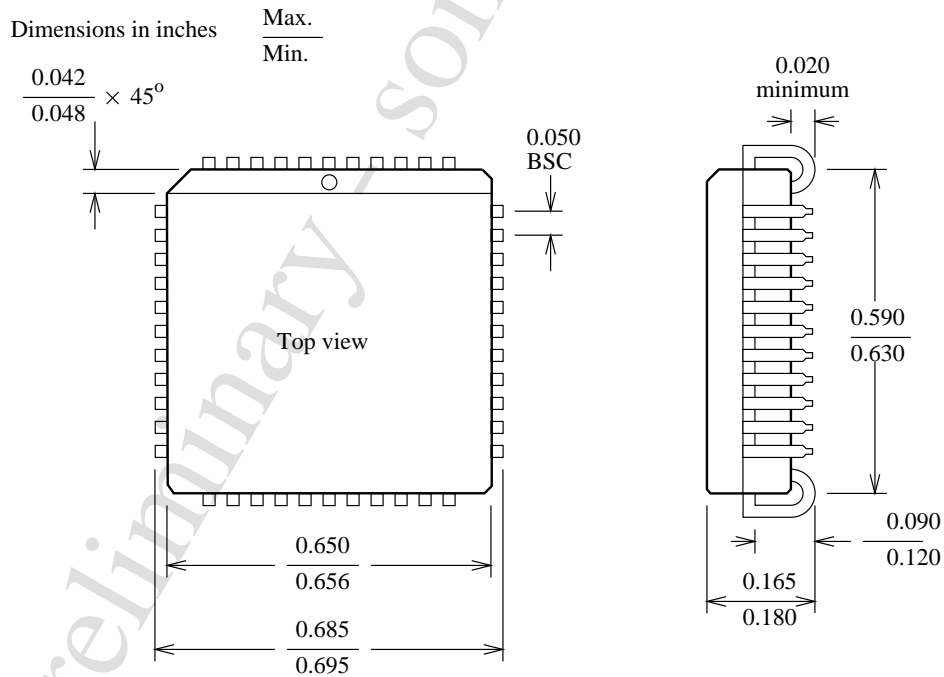
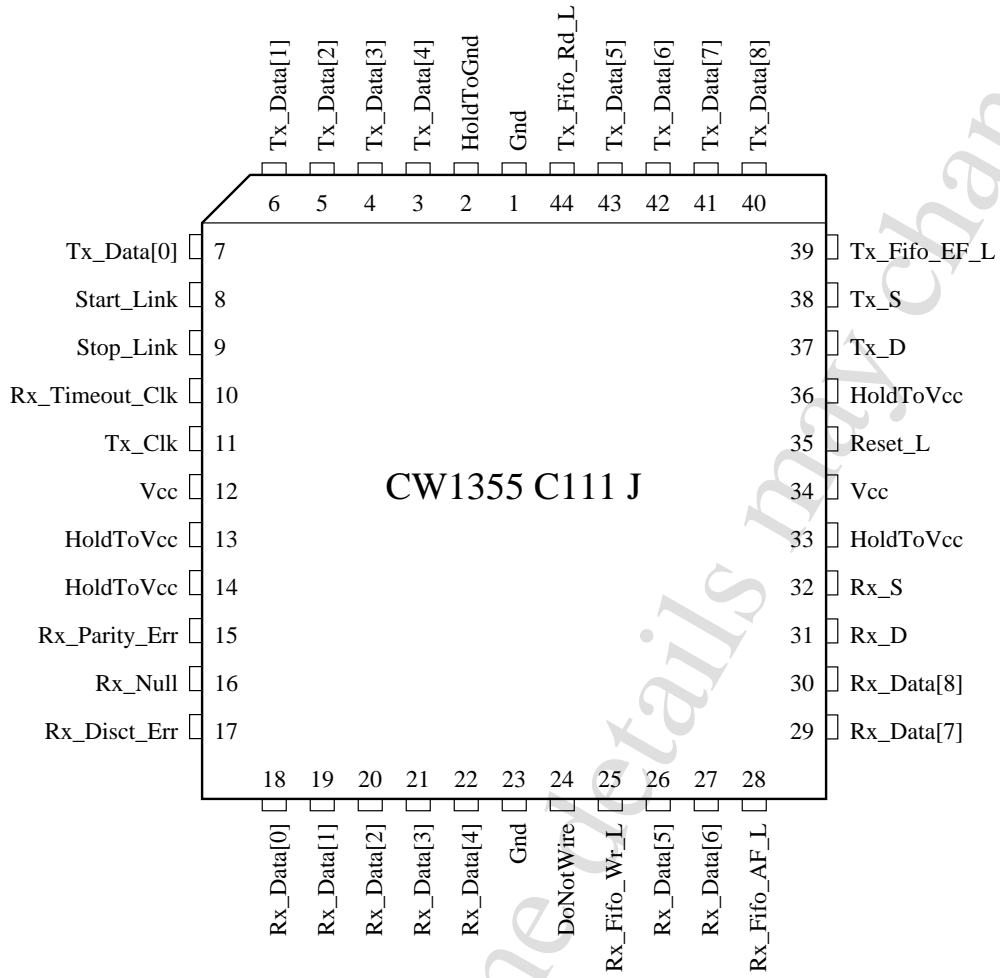
# Application Examples

Fuller descriptions of these circuits and other information is contained in the associated application notes.

## Transmit and Receive both buffered with FIFO's

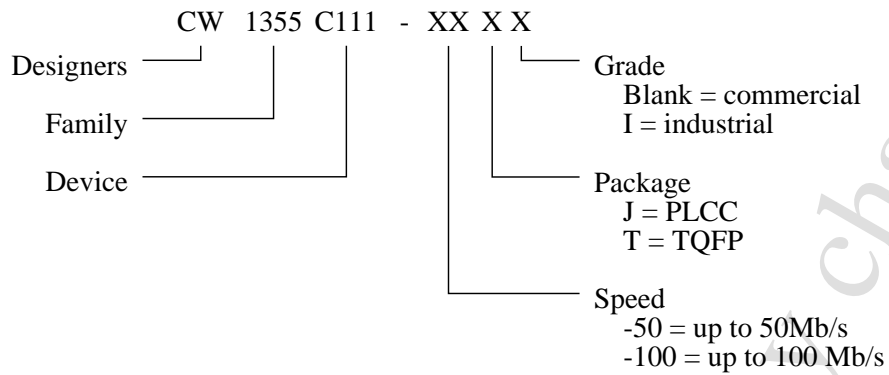


# Pin Configuration - 44pin PLCC package



Last revised: 8<sup>th</sup> November 1996

# Part Number Description



## Ordering Information

### Commercial

Max data rate (Mb/s)	Ordering Number	Package
50	CW1355 C111 - 50 J	44-Pin PLCC
100	CW1355 C111 - 100 J	44-Pin PLCC

### Industrial

Max data rate (Mb/s)	Ordering Number	Package
50	CW1355 C111 - 50 JI	44-Pin PLCC

Contact 4Links for TQFP information.

---

This document describes devices in development, final versions may differ in one or more respects from the information given here. We reserve the right to change specifications or to discontinue products without notice. We do not assume any liability arising out of the application or use of any product, nor do we convey any licence under our patent rights or the rights of others. This product is not designed, intended, authorised or warranted to be suitable for use in life-support devices or systems.